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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,868	06/05/2000	Gordon Caruk	0100.0000430	7484

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EXAMINER	
KING, JUSTIN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,868	CARUK ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6 and 8-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3-6,8-20,40,44 and 45* is/are allowed.

6)☒ Claim(s) *21-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 21-22 are objected to because of the following informalities: The claim 21's second limitation recites "internal circuit", and the claim 22's last line recites "internal I/O circuit". Applicant may have meant "on chip circuit" and "on chip I/O circuit". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 21-23 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melo et al. (U.S. Patent No 6,040,845) in view of Langendorf (U.S. Patent No. 6,624,817).

Referring to claim 21: Melo discloses an internal circuit (figure 1, structure 12) receiving a bus bridge signal from a internal bus bridge (figure 1, structure 14), and an internal circuit (figure 1, structure 28) arbitrating and controlling the signals from any external circuit (figure 1, structures 32a and 302b) from reaching the internal circuit; thus, Melo's internal I/O circuit prevents signals from any external circuit from reaching the internal circuit. However, Melo does not explicitly disclose or teach the disclosed internal components as on-chip components.

Langendorf discloses a bridge chipset incorporating an AGP controller (figure 2, structure 220, column 4, lines 41-46). Langendorf teaches that it is known to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Langendorf's teaching onto Melo because Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset.

Referring to claim 22: Melo discloses that the external circuit (figure 2, structure 46) receives the bus bridge signal from the internal bus bridge; and the external circuit reflects the bus bridge signal to the internal I/O circuit (figure 2, structure 40).

Referring to claim 23: Melo discloses that the bus bridge has to arbitrate between the graphic signals and the peripheral master signals; thus, the signals been arbitrated and selected is the internal circuit signal, and therefore the bus receives an internal circuit signal from the internal circuit and selects one of the internal circuit signal and the external circuit. Melo further discloses that the internal I/O circuit receives an external circuit signal from the external circuit

(AGP), and the bus bridge also receives the external circuit signal once the arbiter receives and selects the signals.

Referring to claim 25: Melo's internal circuit does not disclose input buffer.

Referring to claim 26: Melo discloses the PCI bus/protocol.

Referring to claim 27: Melo discloses the AGP bus/protocol.

5. Claims 21-27, 29-33, and 35-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Brickford et al. (U.S. Patent No. 6,141,021) in view of Langendorf.

Referring to claim 21: Brickford discloses an internal circuit (figure 1, structure 118) receiving a bus bridge signal from an internal bus bridge (figure 3, combined structures of 114, 124, and 110), and an internal I/O circuit (figure 1, structure 124) arbitrating and controlling the signals from any external circuit (figure 1, structures 120/122) from reaching the internal circuit; thus, Brickford's internal I/O circuit preventing signals from any external circuit from reaching the internal circuit. However, Brickford does not explicitly disclose or teach the disclosed internal components as on-chip components.

Langendorf discloses a bridge chipset incorporating an AGP controller (figure 2, structure 220, column 4, lines 41-46). Langendorf teaches that it is known to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Langendorf's teaching onto Brickford because Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset.

Referring to claim 22: Brickford discloses that the external circuit (figure 3, structures 120/122) receives the bus bridge signal from the internal bus bridge (figure 3, structure 114); and the external circuit reflects the bus bridge signal to the internal I/O circuit (figure 3, structure 124).

Referring to claim 23: Brickford discloses that the bus bridge receiving an internal circuit signal from the internal circuit and an external circuit signal, and selecting one of the internal circuit signal and the external circuit signal; the internal I/O circuit receiving an external circuit signal from the external circuit (figure 3).

Referring to claim 24: Claim 24 is rejected over Brickford and Langendorf as stated above; furthermore, although Brickford does not explicitly disclose multiplexing as the selecting mean, the multiplexing is a well-known selecting practice in the computer art, and Applicant didn't challenge the well-known knowledge of the multiplexer.

Referring to claim 25: Claim 25 is rejected over Brickford as stated above; furthermore, Brickford does not disclose any input buffer.

Referring to claim 26: Brickford discloses a PCI bus protocol (figures 1 and 2).

Referring to claim 27: Brickford discloses an AGP bus protocol (figure 3).

Referring to claim 29: Brickford discloses a computer system including a processing unit coupled to a processor bus, a memory unit coupled to a memory bus (figures 1 and 2), an integrated bus bridge graphics unit (figure 3, combined structures of 114, 124, and 110), coupled to the memory bus and further operably coupled to provide a signal to an external graphic bus (figure 3, the path between structure 122 and the combined structures of 114, 124, and 110), and an internal circuit (figure 3, structure 118) operably configured to avoid signals from the external

graphics bus. However, Brickford does not explicitly disclose or teach the disclosed internal components as on-chip components.

Langendorf discloses a bridge chipset incorporating an AGP controller (figure 2, structure 220, column 4, lines 41-46). Langendorf teaches that it is known to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Langendorf's teaching onto Brickford because Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset.

Referring to claim 30: Brickford discloses that the integrated bus bridge graphics unit is further operably coupled to receive a signal from the external graphics bus via an internal I/O circuit (figure 3, structure 124).

Referring to claims 31-33: Brickford's internal I/O circuit is to select the graphic signal communication from either one of the internal circuit or external circuit. Thus, Brickford discloses that the integrated bus bridge unit is further configurable to select and to provide a signal to one of the internal circuit and the external graphics bus, and is further operably configured to isolate the internal circuit from an external graphic bus signal (figure 3).

Referring to claim 35: Brickford does not disclose any input buffer.

Referring to claim 36: It is the communication's purpose to provide signals uncorrupted by transmission line effects.

Referring to claim 37: Brickford discloses a PCI bus protocol (figures 1 and 2).

Referring to claim 38: Brickford discloses an AGP bus protocol (figure 3).

6. Claims 34, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brickford in view of Langendorf, Kubota (U.S. Patent No. 5,633,599) or being unpatentable over Brickford in view of Langendorf, Chen (U.S. Patent No. 5,850,530).

Referring to claim 34: Brickford discloses that the integrated bus bridge isolates the external signal from the internal circuit (figure 1), but Brickford does not explicitly disclose an input buffer for receiving the external signal. Brickford does not explicitly disclose or teach the disclosed internal components as on-chip components. Langendorf discloses a bridge chipset incorporating an AGP controller (figure 2, structure 220, column 4, lines 41-46). Langendorf teaches that it is known to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset. Kubota discloses a circuit design with a buffer controlled by a selector (figure 4A). Chen discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Langendorf's teaching onto Brickford because Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset, and to adapt Kubota's teaching and the input buffer onto Brickford because Kubota teaches one to enhance the bridge's functionality and performance by I/O buffers, and to adapt Chen's bridge input buffer onto Brickford because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

Referring to claim 41: Brickford discloses a first internal circuit (figure 3, structure 118) operable to provide a first internal signal via a first internal signal path (figure 3, path between the structure 118 and the combined structures of 124, 110, and 114), receiving a first external signal via a first external signal path (figure 3, path between the structure 122 and the combined structures of 124, 110, and 114), a selector circuit (figure 3, structure 124) coupled to the first internal circuit via the first internal path, and to select either the first internal signal or the first external signal. Since Brickford's selector circuit selects signals from either structure 118 or 120/122, Brickford discloses isolating the first internal signal on the first internal signal path from the first external signal.

Brickford does not explicitly disclose or teach the disclosed internal components as on-chip components. Langendorf discloses a bridge chipset incorporating an AGP controller (figure 2, structure 220, column 4, lines 41-46). Langendorf teaches that it is known to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset.

Brickford does not explicitly disclose an input buffer, but the I/O buffer is a well-known practice in the computer art; furthermore, Kubota discloses a circuit design with a buffer controlled by a selector (figure 4A). Chen discloses that it is known to equip the input buffer in the bridge (figures 1-2). Chen discloses that it is known to equip the input buffer to reduce the RETRY signal (columns 1-2). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Langendorf's teaching onto Brickford because Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset, and to adapt Kubota's

teaching and the input buffer onto Brickford because Kubota teaches one to enhance the bridge's functionality and performance by I/O buffers, and to adapt Chen's bridge input buffer onto Brickford because it can reduce the number of RETRY control signals, which will reduce the number of the arbitration attempts.

Referring to claim 42: Brickford discloses a first external circuit (figure 3, structure 122) receives the first external signal via the first external path (figure 3, path between the structures 120 and 110). Since Brickford's selector circuit selects signals from either structure 118 or 120/122, Brickford discloses preventing the first internal signal on the first internal signal path from propagating to the first external signal path when the selector circuit stops the external circuit.

Referring to claim 43: Brickford discloses an AGP card connector (figure 3, structure 120), which is the claimed vacant expansion slot.

7. Claims 28 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brickford in view of Langendorf and Applicant's admitted prior art the NGP protocol or Colton et al. (U.S. Patent No. 4,529,840): Brickford does not disclose the NGP protocol. Both Applicant's disclosed prior art and Colton disclose that the NGP is a well-known industrial practice as an alternative to AGP and PCI at the time applicant made the invention. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Langendorf's teaching onto Brickford because Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset and to adapt NGP onto Brickford because NGP is a known

alternative to the AGP and PCI in designing the computer structure.

Allowable Subject Matter

8. Claims 1, 3-6, 8-20, and 40, 44-45 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

Referring to claim 1: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; a first internal circuit operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; and a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; and an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal; and the second internal circuit is operable to provide the second internal signal via the second internal signal path to both the first internal circuit and the output buffer.

Referring to claims 3-6 and 8-20: Claims are allowed because they incorporate the allowable subject matter from claim 1.

Referring to claims 40 and 44: A configurable AGP interface circuit as structurally illustrated in figures 4 and 5 is structured to include a dedicated output buffer for outputting the internal signal to the add-in AGP card and this internal output signal does not go through the select circuit. The circuit is constructed in the structuring arrangement as the followings; an internal graphics controller operable to provide a first internal signal via a first internal signal path; an input buffer operable to receive a first external signal via an first external signal path; a selector circuit coupled to the internal graphics controller via the first internal sigh path and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal; a bus bridge comprising a bus interface operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

Referring to claim 45: Claim is allowable because it incorporates claim 44's allowable subject matter.

Response to Arguments

10. In response to Applicant's argument that the claimed limitation "internal" is "on-chip" as illustrated in the disclosed Specification (Remark, page 12): In view of Applicant's argument and amendment, the Office Action has been revised in incorporate a new prior art Langendorf.

Langendorf teaches one to reduce power consumption and manufacturing cost by incorporating the AGP controller and the I/O bridge into one chipset.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
December 20, 2005

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/22/05